Invited-01: Manufacturing Technology Solution of Small Via for Heterogeneous Integration.

Dr Yasuhiro Morikawa

Manager, Ulvac Inc.

Here, Smart ICT (Information and Communication Technology) in the 5G era such as "Cloud computing", "Fog/Edge computing" , and Smart Functionalities such as Stand-alone Self-activating MEMS/Sensors construct Smart Systems which enable IoT (Internet of Things), IoE (Internet of Everything) thus Smart Society. Therefore, high-density packaging technologies such as 2.nD, 3D packaging scheme basing on advanced substrate package, WLP (wafer level package) / PLP (Panel level package) as high-density organic interposer (RDL: re-distribution layer), Si interposer and TSV (though silicon via) technologies are among key technologies to satisfy the requirements from the semiconductor devices for 5G/AI (artificial intelligence), and real-time or low latency (< 1ms) devices as "Edge-computing". ULVAC has been continuously developing manufacturing solution technologies to realize the heterogeneous integration SiP by Fan-out (substrate package, WLP / PLP) packaging, Si interposer, TSV and also EMI (Electromagnetic Interference) shielding. In this presentation, buildup multilayer, RDL/Interposer and TSV technologies solutions consisting of plasma etching / ashing and PVD (Physical Vapor Deposition) sputtering to make the high density interconnection package will be introduced.

Invited-02: Market and Technology Trends of Advanced Packaging, Fan-Out Packaging

Mr Favier Shoo

Technology and Market Analyst, Yole Development

In this digital new age, advanced nodes do not bring the desired cost-benefit anymore and R&D investments in new lithography solutions and devices below 10nm nodes are rising substantially. Hence, advanced packaging represents an opportunity to increase product value offering advantages down both the scaling and functional roadmaps. This presentation will focus on arguably one of the most exciting advanced packaging platforms – Fan-Out Packaging. In 2019, key players

from all different business models have Fan-Out packaging solutions in the market. Fan-out packaging technology is not only a bridge to chip-package interaction (CPI) mismatch in pitch size, but is also a viable solution for heterogeneous integration of functionalities, now potentially used for mmWave 5G and Cloud data server applications. Fan-out success is evidently defined by the well-established "core" standard FO market and the startling market penetration of high-density FO (HDFO), which brought Fan-Out Packaging into a whole new level of spotlight.

Invited-03: Highly Accurate, Efficient and Reliable Silicon Photonics Wafer-Level Test and Characterization

Dr Sia Choon Beng

Technical Consultant, FormFactor Inc, Singapore

By 2030, to satisfy the increasing demands for cloud computing and services for various emerging applications such as artificial intelligence, genomics revolution and video transcoding etc, the energy consumption of all data centers is projected to be about 20% of the earth's total energy produced! Silicon photonics with optical fibers is the potential candidate to replace copper interconnects within data centers as it drastically reduce power consumption, cost and size of the optical transceiver modules. By utilising the mature silicon CMOS processing technologies, silicon-based photonics products can be fabricated cost-effectively with well-established production solution. In this invited talk, an optimized and automated setup for optoelectronic test and characterization will be presented. The setup is currently used for known-good-die tests prior to die stacking which is crucial for effective 3DIC heterogeneous integration and packaging of silicon-based optical transceivers. This talk also presents possible solutions to establish challenging correlations of wafer-level tests to the final product tests - as most silicon photonics chips utilize edge couplers to transfer light in and out of the chip in IC packages while most of the commercially available wafer-level test solutions require grating couplers for wafer top-side light transfer.

Invited-04: Reduction of Aging Induced Reliability Degradations Using SAC+X Lead Free Solders

Prof Jeffrey Suhling

Auburn University

Environmental concerns and legislation adopted in Europe and Asia has led to a nearly universal world-wide transition to lead free solders in electronic products over the past 15 years. Most of the lead free solders in use are Sn-Ag-Cu (SAC) alloys. One of the greatest challenges has been that SAC lead free solders are highly susceptible to aging effects, where their mechanical behavior and failure properties degrade with time when exposed to isothermal or variable temperature environments. Such degradations are caused by the unstable microstructures present at very low temperatures, and they can lead to a significant reduction in the reliability of electronic products with time.

In this talk, an overview of our research on the effects of aging on the mechanical behavior of lead free solders is presented. In particular, approaches for mitigating aging effects through the use of additional alloying elements within the traditional SAC alloys will be presented. This work has involved a combination of experimental material characterization and measurements of microstructural evolution, as well as constitutive model development and finite element predictions of reliability. Stress-strain and creep tests have been performed on SAC and SAC+X alloys using miniature tensile samples, and the degradations in the effective elastic modulus, yield stress, ultimate tensile strength, and creep strain rate have been characterized and modeled as a function of aging temperature, aging time, and alloy composition. Analogous results have also been obtained using nanoindentation testing of small solder joints from non-aged and aged lead free electronic assemblies. Finally, cyclic stress-strain testing has been utilized to understand the aging induced degradations in the hysteresis loop and fatigue life.

The results of the experimental mechanical testing have been correlated with observations of microstructural evolution occurring in the SAC and SAC+X lead free solders during aging to develop a fundamental understanding of the causes of the material property degradations. It was found that the coarsening of IMC particles was greatly mitigated in SAC+Bi alloys relative to those observed in the traditional SAC alloys. Immediately after reflow solidification, bismuth rich phases were present in the SAC+Bi joints. During aging at T = 125 C, the bismuth was observed to quickly go into solution both within the beta-Sn dendrites and in the intermetallic rich regions between dendrites. This resulted in solid solution strengthening of the lead free solder. It was also found that the aging-induced presence of bismuth in solution within the beta-Sn matrix provided an increased resistance to the Ostwald ripening diffusion process that coarsens the Ag-Sn IMC particles. The combination of these two effects in the SAC+Bi alloys lead to greatly improved resistance to aging induced effects relative to the standard SAC solder alloys. Finally, we have compared the

time dependent evolution of microstructure with the degradation in strength during aging for both SAC and SAC+X alloys, and good correlations were observed.

Invited-05: Cooling of high-power microelectronic components using flow boiling

Prof Yogendra Joshi

Georgia Institute of Technology

With the continuing trend towards heterogeneous integration, volumetric power densities are likely to increase. Microfluidic two-phase cooling provides a potential solution to achieve high heat transfer capabilities, and high temperature uniformity in the presence of hot spots. This presentation will present an approach for computational simulations of flow boiling for chip cooling, illustrated with multiple examples. Also presented will be experimental validations of the computations.

Invited-06: Development of multi-chip integration non-molded 2.5D IC Packaging Technology

Dr Chen Wei Chung, Curry

Technical Consultant, ASE Global

Recent requirements for 2.5D IC package with high bandwidth and high-performance applications is bringing molded and non-molded 2.5D packaging technology innovations into another level. Our production and development experience in non-molded 2.5D devices include 20 × 20 mm^2 to 70 × 70 mm^2 packages with 2 to 5 chips. Non-molded package has benefits such as cost saving and variable thermal solutions, however the warpage control and stress distribution always become challenges and constraints for larger module hardware. Package design, advanced material selection and process design for stress and warpage control will be illustrated in this presentation. Practical process with reliability results combine with stress simulation data will be discussed as well.

Invited-07: Evolution of Fault Isolation Techniques for Product Failure Analysis

Dr Goh Szu Huat
Deputy Director, GlobalFoundries Singapore

The mission of global fault localization is to narrow the physical inspection area to as small and accurate as possible. This is vital to increase the chance of failure analysis success. Against the backdrop of chip scaling, advanced packaging architectures as well as the prevalence of more complex failure types, conscientious efforts to examine and refine custom fault isolation techniques is crucial to achieve this mission. This talk describes the overall trends in both die and package-level fault isolation techniques. The underlying challenges and motivations that drive these enhancements will also be discussed.

Invited-08: Micro-interconnects: Signal Integrity in 5G Applications

Dr Murali Sarangapani

Senior Principal Research Engineer, Heraeus Materials Singapore Pte Ltd

This presentation deals with two aspects on micro-interconnects in semiconductor packaging. First, recent developments in wire bonding, soldering, sintering primarily designed for low electrical resistivity are reported. Second, these wire-bonded, sintered and soldered structures satisfy low loss in transmitting wide bandwidth signals in 5G applications are discussed.

In bonding wire technology, bare and palladium coated copper wires have positioned themselves in high volume replacing gold bonding wires successfully. Alloyed silver wires are used in LED. Gold coated silver wires are studied for memory applications using cascade bonding method. Low temperature bismuth-tin solders have been examined for the last few decades and currently are popular in the usage to reduce warpage (zero) and electrical power consumption. The reflow temperature of these solders are aimed to be less than 190°C. Sintering with nanoparticles reduces process temperature by rapid necking. Using bi-modal electrically conductive powder particles and

composite materials, Heraeus-innovation team explores sintered interconnects to process with low reflow/sinter temperatures. In addition, the sintered interconnects possess low insertion losses with good signal and power integrity. The talk concludes with a challenge to researchers to develop new interconnect materials without limiting the boundaries between electrical resistivity and high-volume production, while still aiming to innovate micro-interconnects with unified performance that blends signal integrity with low insertion loss and low electrical/thermal resistivity.

Invited-09: Development of Novel Polymer Materials for Advanced Packaging

Dr Takenori Fujiwara
Senior Research Associate, Toray Industries

The advanced packaging market will grow dramatically. Advanced packages will continue their important role of addressing high-end logic and memory in computing and telecom, with further penetration in analog and RF in high-end consumer/mobile segments. All of this while eyeing opportunities in the growing automotive and industrial segments.

To fulfil next-generation hardware performance requirements, advanced packaging must press for innovations in process, materials, and equipment. Indeed, advanced packaging has accelerated the need for breakthrough technologies in substrate manufacturing, package assembly, and test engineering. As for materials, there is a desire to develop new dielectric materials, mold compounds, underfill (including Non-conductive film(NCF), solder interconnects.
Temporary Bonding De-Bonding materials (TBDBs) and thermal interface materials (TIMs) for fulfilling the stringent performance and reliability requirements demanded by next-generation hardware. Also, the need for breakthroughs in package feature-scaling requires a sense of urgency from key suppliers to the semiconductor packaging industry.
This report covers the trends and challenges specific to advanced packaging materials technology, and includes detailed technical roadmaps for various packaging materials based on our materials.

Invited-10: Virtual prototyping for electronic packaging development, dream or reality
-Bridging the gap between Simulation and Reality in electronic packaging

Dr Jing-En Luan

R&D Manager, ST Electronics

New product or module development is very challenging nowadays. The development cycle time is shortening, and reliability requirement is higher and higher. CAE is widely used in package development. Simulation become more and more important in new product development. Industry is pursuing virtual prototyping for new product.

However, the accuracy of the models and simulation results is one of the biggest limitations that virtual product development engineers have today. in the product or package development team, there is always challenging and argument how to use simulation results. Engineers from different background have different opinions. The PM/ EPM may have difficulty to understand or believe the results.

In the presentation, the author will share the product/package development flow. The key milestones during development. And how modeling supports it for virtual prototype and key limitation. The author will share examples on each key area to bridge the gap between simulation and experiment or reality.

Virtual prototyping is possible with improvement in key area while designer/simulation engineer/material test / engineer work together. It make a higher level of integration not only engineering but also manpower.

Invited-11: A comprehensive Reliability assessment on 2.5D and 3D Integration

Mr Premachandran CS

Senior Member of Technical Staff, Globalfoundries (USA)

Prem (Premachandran,CS) holds a Master's degree in Engineering from Indian Institute of Technology (IIT), Chennai, India and is currently working in GLOBALFOUNDRIES, Malta, NY. He has published more than 70 publications in journals/conferences,holds more than 25 patents awarded/pending and has co-authored an engineering book in MEMS Packaging. He has given invited talk and tutorials in EPTC, ECTC and IRPS conferences. He is a senior member of IEEE and has session chaired in many conferences and has received a best paper award in IITC 2014.

System level integration on logic and memory has been an important subject to packaging community for mobile and HPC(High performance computing) applications. Recent years, 3DIC integration technology has advanced from substrate level package to wafer level system integration. Wafer level integration leads the semiconductor industry into a new era of system scaling beyond Moore's Law. This talk will give the requirement of reliability aspects on 3D fine pitch wafer to wafer bonding and 2.5D interposer on 65nm technology which is set to go on volume production.

Invited-12: System Packaging Solutions for High Performance Computing in the Era of 5G/IoT

Mr. Shunichi Kikuchi

Corporate Vice President, Fujitsu Advanced Technologies Limited

High Performance Computers have been extending the performance in order to computationally solve intensive tasks in various fields, combining a variety of packaging technologies. The transition in their performance can be seen in the past ToP500 lists. The list which discloses High Performance LINPACK (HPL) benchmark scores from No.1 to No.500 is updated twice a year. Through the data analyses of the past ToP500 lists in the past 26 years, several findings and current trends from the viewpoint of system packaging can be shared with audience. With processor packaging trends, high

speed interconnects and other promising technologies, a few system packaging solutions will be introduced for future high-performance computing. Moreover, I will also explain about newly prepared measurement methods in order to implement the above system packaging. Finally, I will present a direction of system packaging for the era and beyond, including challenges facing the sustainable development goals.

Invited-13: Plasma process optimization for Cu bonding integration using the design of experiment technique

Prof Sarah Kim

Seoul National University of Science and Technology

The vertically stacked devices called 3D integrated circuit packaging have been focused to realize an extreme miniaturization, a cost reduction and more functionality. Among three core processes in 3D IC packaging, a wafer bonding process is still an immature process for D2W mass production compared to TSV and wafer thinning process. Especially with the demand of fine-pitch interconnection, Cu bonding is of great interest in 3D IC heterogeneous packaging. In this study, a low temperature Cu bonding is evaluated with the formation of copper nitride passivation layer, which its optimization was carried out by the design of experiment technique. The bonding quality by SAT measurement, 4PB measurement, and SEM measurement and the lifetime reliability of nitride passivation layer will be discussed.

Invited-14: Novel MEMS based Lateral Contact Probing Method for Fine Pitch Micro-bumps for High Bandwidth Memory (HBM) Testing

Venue: 3911 Date/Time: 6/Dec/19, 9:00am – 9:30am

Dr Daniel Rhee Min Woo

Program Manager, Samsung Korea

The conventional pre-bond testing method operates probes vertically on micro-bumps, and the contacted tip end of the micro-bumps inevitably gets damaged. This is detrimental to the IC assembly, which is the post-testing stage, because it causes a defective junction problem. To overcome this problem, we proposed lateral contact probing of fine pitch micro-bumps because it does not damage the tip end of the micro-bumps at all. We successfully demonstrated the testing, for the first time, with monolithically fabricated fine pitch probes. In addition, whereas conventional probes require a very complicated fabrication process for high flexibility to reduce the damage to the micro-bumps, another feature in this work is that the probes do not need high flexibility or complex fabrication. Thanks to the simple structure of the probes for the lateral contact, the fabrication is designed with only one thick negative PR mold and nickel electroplating to construct it all. The fabricated probes were laterally driven as much as 7μm without plastic deformation, which is acceptable considering the error in the plane direction of chips. In addition, the tested probes were repeatedly driven 5μm for 100,000 cycles and their CCC was at least larger than 180 mA. With these probes, we successfully demonstrated contact without degradation on the tip end of the micro-bumps and the measured contact resistance was 1.13, the highest. All the side-walls of the micro-bumps showed low damage regardless of the material. Moreover, about 10,000 probes were uniformly fabricated in a batch process. By employing the proposed concepts with all the results we had, we expect this lateral contact probing method is a prospective solution for pre-bond testing of modern advanced fine-pitched micro-bumps.

Invited-15: Importance of Warpage Engineering in the era of Heterogeneous Integration

Prof SB Park

State University of New York at Binghamton

As Moore's law is being challenged by increased cost and physical limitations, many forms of SIP (System in Package) including Heterogeneously Integrated Packages are rising as alternative solutions and practical breakthrough. Regarding SIP, naturally, the deformation of a package and

its assembly become more complicated. The need for through understanding its behavior is ever increasing for higher yield in manufacturing as well as better reliability for operation. In this presentation, a method that makes modeling more reliable and dependable is introduced with some case studies. Starting from the detailed material characterization, adjustment of the measured properties, and confirmation of the effectiveness by the measured warpage are included. In addition, 3D-DIC, a new method of quantifying the deformation of a package during reflow, is introduced.

Invited-16: Material Advancement for Heterogenous Integration

Dr Dongshun Bai

Director, Brewer Science

Heterogenous integration (HI) has increasingly attracted attention in the semiconductor industry. In HI, separately manufactured components with different materials, sizes, thicknesses, functionalities, and process technologies can be integrated into a higher-level system to provide enhanced functionality and improved operating characteristics. HI needs new materials in semiconductor, conductor, dielectric, molding, and die-attach applications. Through rational structural design, we can control many physical and chemical properties of the materials to achieve the desired performance. In this talk, new material development at Brewer Science for HI will be introduced. The approach for innovative material design and specific examples including new temporary bonding and debonding materials, novel permanent materials, and materials for adhesion promotion and copper protection applications will be presented.

Invited-17: Innovative Package Solution for 5G Era

Dr. Yu-Po, Wang

Director, SPIL Corporate R&D Centre

In 1997, he started career at Gintic Institute of Manufacturing Technology in Singapore. He has jointed SPIL since 1998 and led the R&D advanced packaging design team for leadframe, substrate and wafer form packages development.

Dr. Wang has strong knowledge and experience in packaging characterization including thermal/ electrical simulation, advanced material(co-development), design and advanced packaging development. He has 83 patents in US. Dr. Wang has strong knowledge and experience in packaging characterization including thermal/ electrical simulation, advanced material(co-development), design and advanced packaging development. He has 83 patents in US.

Invited-18: Memory-Centric Design Challenges for Flash products

Dr Gokul Kumar

Senior Manager, Package Design and Development, Micron

Dr. Gokul Kumar has around ten year's cumulative experience in electronic packaging. He has a multi-disciplinary background encompassing package design, physical design/layout, signal/power integrity, substrate fabrication, technology validation and product development. He currently serves as a Principal Engineer with Western Digital, USA. In this capacity, he has championed several key contributions to Flash Memory and Memory-centric ASIC products over the last 5 years.He has co-authored over 15 journal and conference publications, which have been cited over 450 times. He also has 5 United States Patents in the area of memory-logic integration. In addition, Dr. Kumar is a peer reviewer for a number of internationally reputable conferences and journals. He has also served on several technical panel committees, in addition to being the technical invited speaker at the IEEE Electronics Packaging Technology Conference for the last couple of years.

Co-integration of logic and memory stacks (both DRAM and NAND) into extremely miniaturized packages has been at the forefront of mobile and consumer semiconductor innovation. With the recent advent of 5G and other data-centric design applications, this has created several opportunities for exponential growth. However, the challenges from 3-D NAND and DRAM co-integration have also posed several design bottlenecks in achieving low-cost packages that meet electrical, thermal and mechanical requirements. This talk will serve to highlight both these

opportunities as well as the package design challenges to be overcome to achieve required performance.

Invited-19: Effects of trace element on electromigration of flip chip interconnect between Cu Pillar and Sn-Bi alloy system

Mr Murayama Kei

Research and Development Consultant, Shinko Electric Japan

From environmental issues, economics and technical points of view, the demands for low temperature soldering is increasing year by year. Sn - Bi solders are powerful candidate materials to realize its demands. We investigated effects of surface finish and trace element on electro-migration of flip chip interconnection between Cu-pillar and Cu or Cu/Ni/Au pad using Sn-Bi solder alloy system by Electron backscattered diffraction (EBSD) and Electron probe micro analyzer (EPMA). We introduce that Au, Pd and Ni trace element influence on electro-migration resistance. Au, Pd atoms play a role of accelerating diffusion Ni into Cu6Sn5. When Au and Pd atoms were small, Inter-metallic compounds growth at Cu pillar side is limited. On the other hand, in case of existing small amount of Ni atoms in solder, they form dense scallop type (Cu,Ni)6Sn5 layer at substrate pad and acted as an effective barrier against diffusion from Cu or Ni pad.

Invited-20: What is new for the fast learning of IC Reliability - Advanced Defect Learning, Package Structural Testing, & Reliability modelling by HPC

Mr Xue Ming

Lead Principal Failure Analysis, Infineon

IC package reliability fails are occurred typically with time, loading stress, and environmental stress, which is often escaped from manufacturing test. Package structural fault is a common early deviations cause reliability failures, for example, wire near short, lifted ball bond, die crack. To learn and implement control in manufacturing process for package structural fault is slow as limited detection and take time with conventional approach. A number of new approach are in our horizon, Package structural fault test, Advanced defect learning, and Reliability modelling with High performance computing. This talk will present to you the state of the art and leading development in this topic.